

RBSP EFW

SOC Software Integration, Verification, and Test Plan RBSP_EFW_SW-005-SOC-001B

Baseline



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Changes

Version	Description
А	Initial Version (Preliminary)
В	Baseline Version Updated EFW SysEng (DWC->MML). Added SDC Lead (MB). Changed QA Lead (RJ -> JF). Updated bug/feature-request tracking discussion and document references.



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1. Introduction

The following document is the integration, verification, and test plan (IVTP hereafter) for the SOC software for the RBSP EFW Instrument. This plan covers both the Command, Telemetry, and Ground Support (CTG, aka. GSE) and Science Data Center (SDC) elements of the EFW SOC. As noted in the RBSP Performance Assurance Matrix (Matrix hereafter; ref [3]), the levels of oversight for instrument flight software (FSW) and SOC/GSE software are radically different (compare tabs 15-17 of ref [3] to tab 14). Because of this radical difference in oversight, the IVTP for FSW and SOC software are described in separate documents.

1.1 Project Definition

The RBSP EFW instrument is composed of four Spin-Plane Electric Field Booms (SPBs), two Axial Electric Field Booms (AXBs) and an Instrument Data Processor Unit (IDPU). The IDPU is responsible for power conversion, boom deployment, sensor electronics, command and telemetry processing. The GSE and SDC software is principally engaged in instrument commanding and data playback, processing, and storage, during all phases of instrument development, integration, and on-orbit operation. While many elements of the software has a great deal of heritage, it is expected that the RBSP EFW SOC and GSE package will be a unique product and will be tested as such.

1.2 Reference Documents

These documents are available on the RBSP EFW ftp site,

Ref	File	Description
[1]	RBSP_EFW_SOC_001_SDP_revB	RBSP EFW SOC Software Development Plan
[2]	7417-9070 APL-RBSP-CDRL_DID-01 rev A	RBSP Contract Plans and Documentation for Science Investigations: CDRL and DIDs
[3]	7417-9096-05_EFW-UCB Instrument Performance Assurance Matrix Rev - 8- 26-08 .xls	« the Matrix »
[4]	RBSP_EFW_SYS_010_SOC_Require ments	RBSP EFW SOC Requirements document.

ftp://apollo.ssl.berkeley.edu/pub/RBSP/

These documents are available on the RBSP EFW ftp site,



2. Integration, Verification, and Test Plan

The EFW SOC IVTP will follow the development plan described in Ref [1], with a detailed integration schedule tied to the milestones contained therein.

As with the EFW FSW, tests of the SOC software will be tied directly to items in the SOC Requirements Document (SOC-RD, [4]) Tracking of test development and validation shall occur in coordination with the SOC-RD, following the example format shown below:

Requirement ID	Description	Verification	Parents	Test Written?	Requirement Verified?
SOC.SDC- 406	Shall provide a mechanism for checking the validity of the current MET<- >UTC conversion at will against the definitive conversion data located at the RBSP MOC during nominal operations.	TEST_406	EFW-533, EFW-534,	<date></date>	<date></date>

If multiple SOC requirements are tested and verified by a given test procedure, that test procedure shall carry a composite name, e.g. TEST_504_607.

Test procedures will be developed by the SDC, and GSE team members, vetted by the EFW SysEng as sufficient for verification purposes, and maintained under configuration control by the EFW System Engineer as per the EFW Configuration Control Plan (RBSP_EFW_PA_010). Consistent with UCB best practices, redlining of test procedures shall be allowed, but so-modified procedures shall be revised and placed under configuration control prior to subsequent use.

Integration, test and verification procedures will be developed consistent with the SOC SDP and the general EFW Integration and Test flow (RBSP_EFW_TE_001). A sufficient set of test cases for each CSCI shall be developed to exercise its functionality and determine its response to contingency events at a given level of integration. These will range from simple sensor excitation and data playback operations as part of the verification of the CTG and NRT modules, to more involved coordinated tests of the PDP module that will involve coordinated acquisition and integration of MOC data products (e.g. EPHEM and ATT data), and EFW sensor and calibration data in order to test and verify the production of quality- and configuration-controlled Level 2 science data products.



Tracking metrics for test and verification are part of the SOC SDP, and include manual collection, tracking, and closure (CTC) of bug reports and feature requests during development, with transition to automated CTC via the "trac" system (<u>http://trac.edgewall.org/</u>) integrated with the EFW SVN repository during Instrument INT.

It is expected that only a limited set of issues that arise with the GSE or SDC will rise to the level of requiring a formal Problem Failure Report (PFR); issues with instrument commanding and L2 data production are the most likely to rise to the level of requiring a PFR for closure.

Consistent with the relevant sections of the UCB EFW Matrix (ref [3]), no formal IV&V process shall be used during the SOC IVT process. UCB best practices, including vigorous software configuration control via SVN shall be used to ensure compliance with the Matrix.

Retesting of previously tested and verified SOC elements due to failure of downstream tests and/or PFRs shall be performed consistent with known dependencies between modules, either functional (command or data paths) or developmental (library).

Consistent with stipulations and limitations outlined in the Matrix, test procedures shall be maintained for inspection, and be made available upon request to APL.